In the Claims:

1-280. (canceled)

281. (new) A process comprising:

A. receiving audible speech;

B. converting the audible speech into digital data representing the audible speech in each of successive ten millisecond frames, for each frame the converting including forming Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data;

C. placing the digital data representing the audible speech for the frames into sequential packets, with each packet having a first stage and a second stage, the placing including:

i. arranging data from a first frame of speech in the primary stage of a first packet; and

ii. arranging data from the first frame of speech in the secondary stage of a second packet, which follows immediately after the first packet, the data in the secondary stage including only Linear Prediction Coding data, Long Term Prediction lag data, parity check data, and adaptive and fixed codebook gain data; and

D. sending the first and second packets of data sequentially over one of a Voice Over Packet network and a Voice Over Internet Protocol network.

282. (new) A process comprising:

A. receiving audible speech;

B. converting the audible speech into digital data representing the audible speech in each of successive ten millisecond frames, for each frame the converting including forming Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data;

C. placing the digital data representing the audible speech for the frames into sequential packets, with each packet having a first stage and a second stage, the placing including:

i. arranging data from a first frame of speech in the primary stage of a first packet; and

ii. arranging data from the first frame of speech in the secondary stage of a second packet, which follows immediately after the first packet, the data in the secondary stage including only Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and a first few of the fixed codebook pulse data; and

D. sending the first and second packets of data sequentially over one of a Voice Over Packet network and a Voice Over Internet Protocol network.

283. (new) A process comprising:

A. receiving audible speech;

B. converting the audible speech into digital data representing the audible speech in each of successive ten millisecond frames, for each frame the converting including forming Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data;

C. placing the digital data representing the audible speech for the frames into sequential packets, with each packet having a first stage and a second stage, the placing including:

i. arranging data from a first frame of speech in the primary stage of a first packet; and

ii. arranging data from the first frame of speech in the secondary stage of a second packet, which follows immediately after the first packet, the data in the secondary stage including Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and all fixed codebook pulse data; and

D. sending the first and second packets of data sequentially over one of a Voice Over Packet network and a Voice Over Internet Protocol network.

284. (new) A process comprising:

A. receiving audible speech;

B. converting the audible speech into digital data representing the audible speech in each of successive ten millisecond frames, for each frame the converting including forming Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data;

C. placing the digital data representing the audible speech for the frames into sequential packets, with each packet having a first stage and a second stage, the placing including:

i. arranging data from a first frame of speech in the primary stage of a first packet, the data including Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and a first set of every other datum of the fixed codebook pulse data; and

ii. arranging data from the first frame of speech in the secondary stage of a second packet, which follows immediately after the first packet, the data in the secondary stage including the Linear Prediction Coding data, the Long Term Prediction lag data, the parity check data, the adaptive and fixed codebook gain data, and a second set of the fixed codebook pulse data not in the first set; and

D. sending the first and second packets of data sequentially over one of a Voice Over Packet network and a Voice Over Internet Protocol network.

285. (new) A process comprising:

A. receiving audible speech;

B. converting the audible speech into digital data representing the audible speech in each of successive ten millisecond frames, for each frame the converting including forming Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data;

C. placing the digital data representing the audible speech for the frames into sequential packets, with each packet having a first stage and a second stage, the placing including:

i. arranging data from a first frame of speech in the primary stage of a first packet, the data including Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, a first few of the fixed codebook pulse data, and a first set of every other fixed codebook pulse datum from the remaining fixed codebook pulse data; and

ii. arranging data from the first frame of speech in the secondary stage of a second packet, which follows immediately after the first packet, the data in the secondary stage including the Linear Prediction Coding data, the Long Term Prediction lag data, the parity check data, the adaptive and fixed codebook gain data, the first few fixed codebook pulse data, and a second set of fixed codebook pulse data from the remaining fixed codebook pulse data and that are not in the first set; and

D. sending the first and second packets of data sequentially over one of a Voice Over Packet network and a Voice Over Internet Protocol network.

286. (new) A process comprising:

A. receiving audible speech;

B. converting the audible speech into digital data representing the audible speech in each of successive ten millisecond frames, for each frame the converting including forming Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data, the forming fixed codebook pulse data including minimizing [error(full rate) + w1 error(Description 1) + w2 error(Description 2)], wherein the letters "w1" and "w2" symbolize weight coefficients, and Description 1 and Description 2 symbolize two descriptions;

C. placing the digital data representing the audible speech for the frames into sequential packets, with each packet having a first stage and a second stage, the placing including:

i. arranging data from a first frame of speech in the primary stage of a first packet, the data including Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and a first set of fixed codebook pulse data; and

ii. arranging data from the first frame of speech in the secondary stage of a second packet, which follows immediately after the first packet, the data in the secondary stage including the Linear Prediction Coding data, the Long Term Prediction lag data, the parity check data, the adaptive and fixed codebook gain data, and a second set of fixed codebook pulse data not in the first set; and

D. sending the first and second packets of data sequentially over one of a Voice Over Packet network and a Voice Over Internet Protocol network.

287. (new) An integrated circuit comprising:

A. first leads receiving speech signals;

B. network leads for sending and receiving packets of digital information that represent speech signals;

C. processor circuitry coupled to the first leads and to the network leads and having memory leads; and

D. memory circuits having processor leads coupled to the memory leads, the memory circuits having bits of information that can operate the processor circuitry, the bits including:

i. converter bits for operating the processor circuitry to convert the speech signals into digital data representing the speech in each of successive ten millisecond frames;

ii. encoding bits for operating the processor circuitry to encode the digital data into Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data for each frame;

iii. packet encapsulation bits for operating the processor circuitry to arrange data from a first frame of speech in the primary stage of a first packet, and to arrange only Linear Prediction Coding data, Long Term Prediction lag data, parity check data, and adaptive and fixed codebook gain data from the first frame in the secondary stage of a second packet.

288. (new) An integrated circuit comprising:

A. first leads receiving speech signals;

B. network leads for sending and receiving packets of digital information that represent speech signals;

C. processor circuitry coupled to the first leads and to the network leads and having memory leads; and

D. memory circuits having processor leads coupled to the memory leads, the memory circuits having bits of information that can operate the processor circuitry, the bits including:

i. converter bits for operating the processor circuitry to convert the speech signals into digital data representing the speech in each of successive ten millisecond frames;

ii. encoding bits for operating the processor circuitry to encode the digital data into Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data for each frame;

iii. packet encapsulation bits for operating the processor circuitry to arrange data from a first frame of speech in the primary stage of a first packet, and to arrange only Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and a first few of the fixed codebook pulse data from the first frame in the secondary stage of a second packet.

289. (new) An integrated circuit comprising:

A. first leads receiving speech signals;

B. network leads for sending and receiving packets of digital information that represent speech signals;

C. processor circuitry coupled to the first leads and to the network leads and having memory leads; and

D. memory circuits having processor leads coupled to the memory leads, the memory circuits having bits of information that can operate the processor circuitry, the bits including:

i. converter bits for operating the processor circuitry to convert the speech signals into digital data representing the speech in each of successive ten millisecond frames;

ii. encoding bits for operating the processor circuitry to encode the digital data into Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data for each frame;

iii. packet encapsulation bits for operating the processor circuitry to arrange data from a first frame of speech in the primary stage of a first packet, and to arrange Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and all fixed codebook pulse data from the first frame in the secondary stage of a second packet.

290. (new) An integrated circuit comprising:

A. first leads receiving speech signals;

B. network leads for sending and receiving packets of digital information that represent speech signals;

C. processor circuitry coupled to the first leads and to the network leads and having memory leads; and

D. memory circuits having processor leads coupled to the memory leads, the memory circuits having bits of information that can operate the processor circuitry, the bits including:

i. converter bits for operating the processor circuitry to convert the speech signals into digital data representing the speech in each of successive ten millisecond frames;

ii. encoding bits for operating the processor circuitry to encode the digital data into Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data for each frame;

iii. packet encapsulation bits for operating the processor circuitry to arrange Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and a first set of every other datum of the fixed codebook pulse data from a first frame of speech in the primary stage of a first packet, and to arrange the Linear Prediction Coding data, the Long Term Prediction lag data, the parity check data, the adaptive and fixed codebook gain data, and a second set of the fixed codebook pulse data not in the first set from the first frame of speech in the secondary stage of a second packet.

291. (new) An integrated circuit comprising:

A. first leads receiving speech signals;

B. network leads for sending and receiving packets of digital information that represent speech signals;

C. processor circuitry coupled to the first leads and to the network leads and having memory leads; and

D. memory circuits having processor leads coupled to the memory leads, the memory circuits having bits of information that can operate the processor circuitry, the bits including:

i. converter bits for operating the processor circuitry to convert the speech signals into digital data representing the speech in each of successive ten millisecond frames;

ii. encoding bits for operating the processor circuitry to encode the digital data into Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data for each frame;

iii. packet encapsulation bits for operating the processor circuitry to arrange Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and a first set of fixed codebook pulse data from a first frame of speech in the primary stage of a first packet, and to arrange the Linear Prediction Coding data, the Long Term Prediction lag data, the parity check data, the adaptive and fixed codebook gain data, and a second set of fixed codebook pulse data not in the first set from the first frame of speech in the secondary stage of a second packet.

292. (new) An integrated circuit comprising:

A. first leads receiving speech signals;

B. network leads for sending and receiving packets of digital information that represent speech signals;

C. processor circuitry coupled to the first leads and to the network leads and having memory leads; and

D. memory circuits having processor leads coupled to the memory leads, the memory circuits having bits of information that can operate the processor circuitry, the bits including:

i. converter bits for operating the processor circuitry to convert the audible speech into digital data representing the audible speech in each of successive ten millisecond frames, for each frame the processor forming Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data, the processor forming fixed codebook pulse data including minimizing [error(full rate) + w1 error(Description 1) + w2 error(Description 2)], wherein the letters "w1" and "w2" symbolize weight coefficients, and Description 1 and Description 2 symbolize two descriptions;

ii. encoding bits for operating the processor circuitry to encode the digital data into Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and fixed codebook pulse data for each frame;

iii. packet encapsulation bits for operating the processor circuitry to arrange Linear Prediction Coding data, Long Term Prediction lag data, parity check data, adaptive and fixed codebook gain data, and a first set of fixed codebook pulse data from a first frame of speech in the primary stage of a first packet, and to arrange the Linear Prediction Coding data, the Long Term Prediction lag data, the parity check data,

the adaptive and fixed codebook gain data, and a second set of fixed codebook pulse data not in the first set from the first frame of speech in the secondary stage of a second packet.